REMARKS

This paper includes a complete and timely response to the non-final Office Action mailed July 15, 2003 (Paper No. 10). Upon entry of the attached amendments, claims 24-46 remain pending. Claims 1-23 have been canceled. Claims 24-46 have been added. The subject matter in new claims 24-46 is included in the circuit embodiments illustrated in FIGs. 3A and 3B and described in the corresponding portion of the specification (page 8, line 27 to page 11, line 16). Consequently, no new matter is added.

Each rejection presented in the non-final Office Action mailed July 15, 2003 is discussed in the remarks that follow.

I. Claim Rejections Under 35 U.S.C. §112 - Claims 1-23

A. Statement of the Objection

Claims 1-23 were rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the written description requirement. Specifically, the statement of the rejection in the Office Action alleges that the claims contain subject matter not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. More specifically, the statement of the rejection alleges that "each said instruction port having a respective self-timed vector logic element" is not supported in the specification.

B. Discussion of the Rejection - Claims 1-23

Claims 1-23 have been canceled without prejudice, waiver or disclaimer. Consequently, Applicant respectfully submits that the rejection of claims 1-23 is rendered moot.

II. Claim Rejections Under 35 U.S.C. §102 - Claims 1-23

A. Statement of the Rejection

Claims 1-23 presently stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by Lesartre *et al.* (U.S. Patent No. 5,761,474, hereafter "the '474 patent.")

B. Discussion of the Rejection - Claims 1-23

Claims 1-23 have been canceled without prejudice, waiver or disclaimer. Consequently, Applicant respectfully submits that the rejection of claims 1-23 is rendered moot.

III. Claim Rejections Under 35 U.S.C. §103 - Claims 1-9 and 13-22

A. Statement of the Rejection

Claims 1-9 and 13-22 presently stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Lesartre *et al.* in view of the Microsoft Computer Dictionary, 4th Edition.

B. Discussion of the Rejection - Claims 1-9 and 13-22

Claims 1-9 and 13-22 have been canceled without prejudice, waiver or disclaimer. Consequently, Applicant respectfully submits that the rejection of claims 1-9 and 13-22 is rendered moot.

IV. Claims 24-46

Applicant's new claims 24-46 are based on claims 1-23 as originally filed. Limitations allegedly unsupported in Applicant's specification are absent from claims 24-46. Claims 24-46 have been added and patently define over the cited art of record in the parent application.

Applicant's independent claim 24 is directed to a method for finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in an instruction reordering mechanism of a processor that can launch execution of instructions out of order. Claim 24 and claims depending therefrom are patentable over the cited art of record for at least the reason that the cited art does not disclose, teach, or suggest "***propagating a set of signals successively through said logic elements of said instruction reordering mechanism, said set of signals responsive to available instruction ports and port information***."

In contrast with Applicant's claimed invention and as indicated in the title of the '474 patent, the system apparently disclosed in *Lesartre* is directed to operand dependency tracking to determine when it is appropriate to execute an instruction in an out-of-order processor. The system of the '474 patent tracks operand dependencies and uses the

dependencies to identify instructions that are ready to be executed. Thus, the system of *Lesartre* is tracking operand dependencies to determine if a corresponding instruction can launch.

Applicant's disclosure is directed to an instruction reordering mechanism that tracks allocated ports for launching instructions ready to launch (*i.e.*, instructions in slots of the reordering mechanism have no dependency conflicts). Applicant's claimed method is directed to the propagation of port availability via a set of signals. Propagation of port availability via a set of signals is not tracking operand dependencies to identify if an instruction can launch. Consequently, claims 24 through 32 are allowable.

Applicant's independent claim 33 is directed to a method for quickly finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in a queue of a processor that can launch the execution of instructions out of order, so that the found instructions can be communicated to a corresponding predefined plurality of ports associated with one or more execution resources. Claim 33 and claims depending therefrom are patentable over the cited art of record for at least the reason that the cited art does not disclose, teach, or suggest "***propagating a set of signals successively through slots of said queue during a launch cycle, said set of signals responsive to available instruction ports and port information to launch execution of an instruction*** . . ."

As shown above, the cited art of record fails to disclose, teach, or suggest Applicant's claimed limitation. Consequently, claims 33 through 35 are allowable.

Applicant's independent claim 36 is directed to a system for finding a predefined plurality of instructions, if available, that are ready to be executed in a processor that can launch execution of instructions out of order. Claim 36 and claims depending therefrom are patentable over the cited art of record for at least the reason that the cited art does not disclose, teach, or suggest "a plurality of logic elements associated with said instruction reordering mechanism and associated respectively with each of said instructions in said instruction reordering mechanism for causing and preventing launching, when appropriate, of respective instructions, ***said logic elements configured to propagate a plurality of signals through said logic elements, said plurality of signals responsive to available instruction ports and port information*** . . ."

As shown above, the cited art of record fails to disclose, teach, or suggest Applicant's claimed limitation. Consequently, claims 36 through 45 are allowable.

Applicant's independent claim 46 is directed to a system for finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in a queue of a processor that can launch execution of instructions out of order. Claim 46 is patentable over the cited art of record for at least the reason that the cited art does not disclose, teach, or suggest "logic means associated with said queue, ***said logic means for propagating a set of signals to successive launch logic means, said set of signals responsive to available instruction ports and port information*** . . ."

As shown above, the cited art of record fails to disclose, teach, or suggest Applicant's claimed limitation. Consequently, claim 46 is allowable.

CONCLUSION

In summary, Applicant's cancellation of claims 1-23 has rendered the corresponding multiple rejections of these claims moot. Applicant respectfully submits that new claims 24-46 are allowable over the cited art of record and the present application is in condition for allowance. Accordingly, a Notice of Allowance is respectfully solicited. Should the Examiner have any comments regarding the Applicant's response, Applicant requests that the Examiner telephone Applicant's undersigned attorney.

Respectfully submitted,

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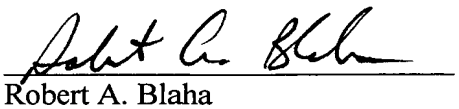
By: 
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